

**9020 D System
9020 E System
Design Data**

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International Business Machines Corporation

APPENDIX C. EXAMPLE OF MICROPROGRAM CONTROL

The following is an example of the microprogram control required to perform a machine instruction. The instruction chosen is an Add which will add a 32-bit binary word from storage to a 32-bit word in a General Register and place the sum in that General Register. Indexing is used in computing the storage address. The instruction will take the form:

(RX) 5A R₁ X₂ B₂ D₂

Where: 5A is the Op Code

R₁ specifies the General Register whose contents will be added to the word from storage and which will receive the sum.

X₂ defines the Index Register to be used.

B₂ defines the Base Register to be used.

D₂ is the Displacement Address.

Each micro-instruction represents a 0.2-usec machine cycle. Figure C-1 shows machine actions. Only major actions are shown.

The first micro-instruction related to this instruction occurs as part of the previous instruction executed. Since instructions are fetched by doublewords, the Q register may contain up to four instructions at a time. Consequently, the address calculation for the second operand of the 5A instruction may be initiated early by accessing the B₂ field of the next instruction in the Q register.

Micro-instructions 1 and 2 provide a common RX format I-fetch when X₂ ≠ 0 and B₂ ≠ 0. These instructions compute the address of the second operand and make a storage request. Additionally, the next instruction is accommodated by updating the instruction counter and placing the first halfword of the next instruction in the R register for prefetching of operands.

The next three micro-instructions provide a common fixed point operand fetch operation.

The sixth micro-instruction is the execute cycle for a fixed point Add instruction. The results are placed in local store and exceptional conditions are tested.

The final micro-instruction for Op Code 5A is a common End Operation which sets applicable condition codes and provides operand prefetch for the following instruction.

The microprogramming shown in Figure C-1 has been simplified for clarity in presentation. It is representative of the micro-routine required to execute a typical machine instruction.

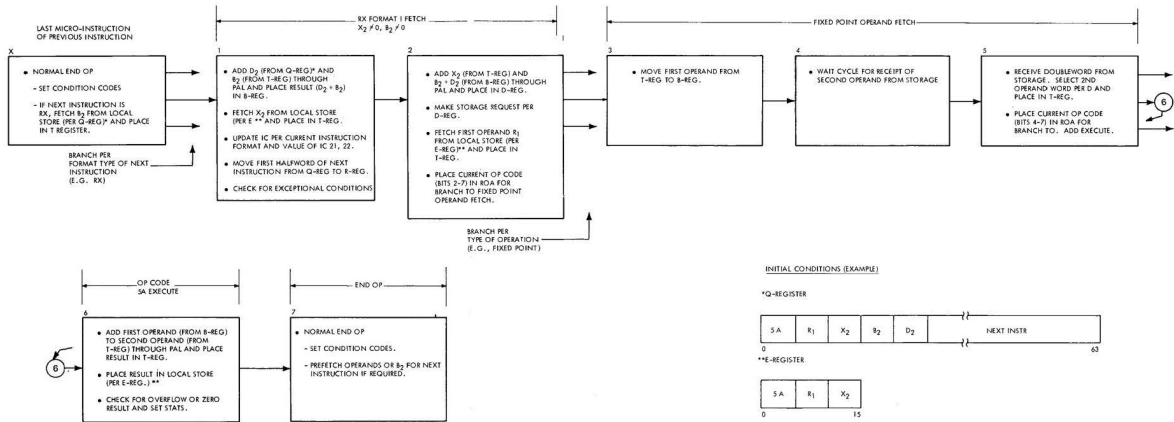


Figure C-1. Microprogram Control of Add Instruction